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SDRAM and CAS latency and FIFO

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1. Dual-bank **FIFO** for synchronization of read data in DDR **SDRAM** ...

Dual-bank **FIFO** for synchronization of read data in DDR **SDRAM**. Document Type and Number: The value is normally based on the DRAM **CAS latency**. ...

www.freepatentsonline.com/6920526.html - [Similar pages](#)

by MR Sikkink - 2005 - [Cited by 1](#) - [Related articles](#) - [All 3 versions](#)

2. **SDRAM latency** - Wikipedia, the free encyclopedia

Dec 8, 2008 ... tCAS: The number of clock cycles needed to access a certain column of Data in **SDRAM**. **CAS Latency**, or simply **CAS**, is known as Column Address ...

en.wikipedia.org/wiki/RAM_latency - 25k - [Cached](#) - [Similar pages](#)

3. Dual-bank **FIFO** for synchronization of read data in DDR **SDRAM** ...

The present invention comprises a dual bank **FIFO** memory buffer operable to buffer ... periods through the **SDRAM(CAS latency)**; a DQS flight time back to the ...

www.patentstorm.us/patents/6920526/description.html - [Similar pages](#)

4. **CAS Latency**

Nov 1, 2000 ... In that case the RAS to **CAS latency** can be 2 or 3 clock cycles, depending on the quality of the **SDRAM**. If the chipset has left open a ...

www.dewassoc.com/performance/memory/cas_latency.htm - 12k

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5. Streaming Multi-port **SDRAM** Memory Controller

You can also configure port **FIFO** buffer depth (from 16 to 2048 bytes) to the ... **CAS latency** overhead encountered using a short burst access controller. ...

www.altera.com/products/ip/iup/memory/m-mtx-stream-sdram.html - 39k

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6. Tech ARP - **SDRAM CAS Latency Time**

Therefore, while it is recommended that you reduce the **SDRAM CAS Latency** Time to 2 or 2.5 clock cycles for better memory performance, you should increase it ...

www.techarp.com/showfreebog.aspx?lang=0&bogno=190 - 39k

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7. [\[PDF\] Xilinx XAPP867 High-Performance DDR3 **SDRAM** Interface in Virtex-5 ...](#)

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SDRAM devices also support posted **CAS** additive **latencies**; these allow a Read or The backend user interface has three FIFOs: the Address **FIFO**, the Write ...

www.xilinx.com/support/documentation/application_notes/xapp867.pdf - [Similar pages](#)

8. [DDR **SDRAM** DIMM interface for Virtex-II devices](#)

asserted by the USB controller, and the ddr_ae (**FIFO** almost empty) is asserted.

The cas_lat bit sets the **CAS latency** for the DDR **SDRAM** device. ...

www.eetindia.co.in/ART_8800383431_1800009_AN_87f6221b.HTM - 108k

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9. [\[PDF\] A 2.5-ns Clock Access, 250-MHz, 256-Mb **SDRAM** with Synchronous ...](#)

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clock frequency of **SDRAM** has been rapidly increased from. 125 MHz [1] to 200 MHz [2], The **FIFO** consists of five registers for **CAS latency**. (CLT) = 5. ...


sscs.org/jssc/96bp.pdf - [Similar pages](#)

10. [\[PDF\] TBR-Riedl Generic **SDRAM** Controller VHDL Core](#)

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to connect different microprocessor interfaces, **SDRAM** based **FIFO** controller or ... All access timing parameters such as **CAS latency**, row-to-column delay, ...

www.tbr-riedl.de/Produkte/Memory_Controller/tbr_sdram_ctrl_pn.pdf - [Similar pages](#)

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1. [A 6-ns 256-kb BiCMOS TTL **SRAM** - Solid-State **Circuits**, IEEE Journal of](#)

Output Buffer. A two-level-presetting **circuit** controls the **rise** and the **fall**. of data outputs. four common input/**output** pins. The fabricated **SRAM**'s ...

[ieeexplore.ieee.org/iel1/4/2493/00075033.pdf?arnumber=75033](#) - [Similar pages](#)
by T Akioka - 1991 - [Cited by 3](#) - [Related articles](#) - [All 2 versions](#)

2. [A 3.3-V 12-ns 16-Mb CMOS **SRAM** - Solid-State **Circuits**, IEEE Journal of](#)

the delay and **output rise/fall** time with SPICE by chang- the 16-Mb **SRAM**. It has all the peripheral **circuits** and bond pads in the cen- ...

[ieeexplore.ieee.org/iel1/4/4254/00165327.pdf?arnumber=165327](#) - [Similar pages](#)
by H Goto - 1992 - [Cited by 10](#) - [Related articles](#) - [All 5 versions](#)
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3. [Multiplexed **output circuit** and method of operation thereof - US ...](#)

Consequently, the **rise/fall** control normally required in **output** buffers of static random access memory (**SRAM**), includes memory arrays 502, 504 ...
[www.patentstorm.us/patents/5867053/description.html](#) - [Similar pages](#)

4. [Control **circuit** having outputs with differing **rise** and **fall** times ...](#)

pull down transistor has a fast **fall** time and slow **rise** time with respect to the input signal. When the control **circuit** is used for controlling a static **RAM** ...
[www.patentstorm.us/patents/5187686.html](#) - [Similar pages](#)

5. [Multiplexed **output circuit** and method of operation thereof ...](#)

Output buffer 120 often includes a **rise/fall** control 121 to introduce **rise** time and **fall** Memory 500, for example a static random access memory (**SRAM**), ...
[www.freepatentsonline.com/5867053.html](#) - [Similar pages](#)
by BE Engles - 1999 - [Cited by 1](#) - [Related articles](#) - [All 3 versions](#)

6. Cycle independent data to echo clock tracking **circuit** - Patent 6134182

Data from the **SRAM** array 10 is divided into two groups, **rise** data and **fall** data. The **rise** data is latched through to a microprocessor input buffer (not ...

www.freepatentsonline.com/6134182.html - [Similar pages](#)

by H Pilo - 2000 - [Cited by 4](#) - [Related articles](#) - [All 3 versions](#)

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7. [PPT] CSE477 VLSI Digital **Circuits Fall** 2002 Lecture 24: **RAM** Cores

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CSE477 VLSI Digital **Circuits Fall** 2002. Lecture 24: **RAM** Cores Q point doesn 't **rise** too high before Cbit is discharged or the memory cell will change ...

bwrc.eecs.berkeley.edu/ICBook/Slides/PennState/cse477-24%20mem%20cores.ppt

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8. Semiconductor integrated **circuit** controlling **output** impedance and ...

Sep 4, 2008 ... An **output circuit** comprising plural **output** MOSFETs connected in parallel is used , ... and **rise/fall** time changes depending on conditions. ...

www.freshpatents.com/Semiconductor-integrated-circuit-controlling-output-impedance-and-slew-rate-di20080904ptan200802... - 27k - [Cached](#) - [Similar pages](#)

9. Chapter 2: Verilog Structure

In Verilog, **circuit** components are designed inside a module. The delay operator can also use the full **rise**, **fall**, and off delays and each delay can ...

www.verilogtutorial.info/chapter_2.htm - 17k - [Cached](#) - [Similar pages](#)

10. ASIC-System On Chip (SoC)-VLSI Design: Short **Circuit** Power

Short **circuit** currents are significant when the **rise/fall** time at the input of a gate is much larger than the **output rise/ fall** time. ...

asic-soc.blogspot.com/2008/04/short-circuit-power.html - 232k

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